WHAT IS CLAIMED IS:

1. A computer system comprising:

a digital signal processing (DSP) core for processing data in accordance with an instruction;

a data cache for storing temporary data associated with the DSP core;

a first buffer module for storing input data received by the DSP core;

a second buffer module for storing output data provided from the DSP core; and

an external memory for storing the temporary data, the input data, and the output data.

2. The computer system of claim 1, wherein the first and second buffer modules comprise:

an address buffer for storing an address of the external memory;

an increment unit for increasing the address by one bit;

a buffer for storing either the input data or the output data; and

a multiplexer for addressing the buffer in response to lower bits of the address.

3. The computer system of claim 2, wherein the address of the external memory is initialized by a central processing unit (CPU) core.

4. The computer system of claim 2, wherein the buffer comprises a set of data registers.

5. The computer system of claim 2, wherein the buffer comprises valid bits that inform of current occupation state by data in the data registers.

6. The computer system of claim 1, wherein the external memory comprises a temporary data field, an input data field, and an output data field which are independently arranged therein.

7. The computer system of claim 2, wherein when the buffer is empty, a CPU core carries out a pre-fill operation to serially read the input data from the external memory and stack the input data in the buffer.

8. The computer system of claim 2, wherein when the buffer is full, a CPU carries out a post-flush operation to store the output data of the buffer in the external memory.

9. The computer system of claim 2, wherein an auto-fill operation is carried out by the buffer module to stack the input data of the external memory in the buffer when the buffer is empty.

10. The computer system of claim 2, wherein if the buffer is full, the buffer module carries out an auto-flush operation to store the output data of the buffer in the external memory.

11. The computer system of claim 1, wherein the computer system is

integrated on a chip, comprising a CPU core, the DSP core, the data cache, and the first and second buffer modules.

12. A method of accessing data in a computer system having a digital signal processing (DSP) core, a data cache, a buffer, and an external memory, comprising the steps of:

accessing temporary data for the external memory through the data cache if data of the DSP core includes the temporary data;

executing a pre-fill operation to serially transfer input data to the buffer when the buffer is empty;

executing a post-flush operation to store output data of the buffer in the external memory when the buffer is full;

executing an auto-fill operation to stack the input data of the external memory in the buffer when the buffer is empty; and

executing an auto-flush operation to store the output data of the buffer in the external memory when the buffer is full.